



QJO Series

SMD Oscillator, 9x14x4.7mm, LVPECL / LVDS

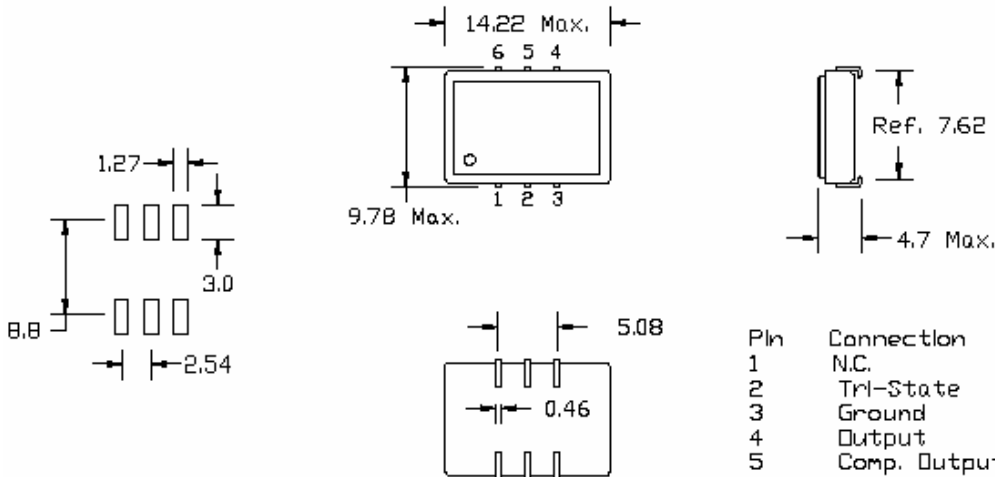
Frequency	1.000 MHz to 750.000 MHz	
Output Level	LVDS	PECL
Level	Vod = 393 mV Typ., 475 mV Max.	'0' = Vcc-1.63 VDC '1' = Vcc - 1.02 VDC Min. Max.
Duty Cycle	Specify 50% ± 10% or ± 5% See Table	
Rise / Fall Time	0.6 nS Max.	
Output Load	100 Ω Differential	50 Ω to Vcc - 2.0 VDC
Frequency Stability	See Frequency Stability Table (Includes room temperature tolerance and stability over operating temperature)	
Start-up Time	10 mS Max.	
Enable / Disable Time	100 nS Max.	
Supply Voltage	3.3 VDC ±10%	
Current	130 mA Max. **	
Temperature		
Operating	See Operating Temperature Table	
Storage	-55° C to +125° C	
Environmental / Tape and Reel	See Application notes for Environmental information for Tape and Reel information	
Package Information	MSL = N.A., Termination = e4	

Part Number Guide		Sample Part Number:		QJO-3ATA1T-156.250 MHz			
Package	Input Voltage	Operating Temperature	Symmetry (Duty Cycle)	Output	Stability (in ppm)	Enable / Disable	Frequency
QJO-	3 = 3.3 V	A = 0° C to +70° C	T = 45 / 55 Max.	A = LVDS	1 = ± 100	H = Enable	- 156.250 MHz
		B = -10° C to +70° C	S = 40 / 60 Max.	B = PECL	2 = ± 50		
		C = -20° C to +70° C			3 = ± 25		
		D = -30° C to +75° C			4 = ± 20		
		E = -40° C to +85° C			*5 = ± 15		

NOTE: A 0.01 μF bypass capacitor is recommended between Vcc (pin 6) and GND (pin 3) to minimize power supply noise.

* Not available for all temperature ranges.

** Frequency, supply, and load related parameters.



Pin	Connection
1	N.C.
2	Tri-State
3	Ground
4	Output
5	Comp. Output
6	Vcc

Tri-State Function	
Pin 2 Open	Enable
Pin 2 70% Vdd	Enable
Pin 2 30% Vdd	Disable

Dimension Units: mm

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Specifications subject to change without notice (Rev A)